

FIG. 1

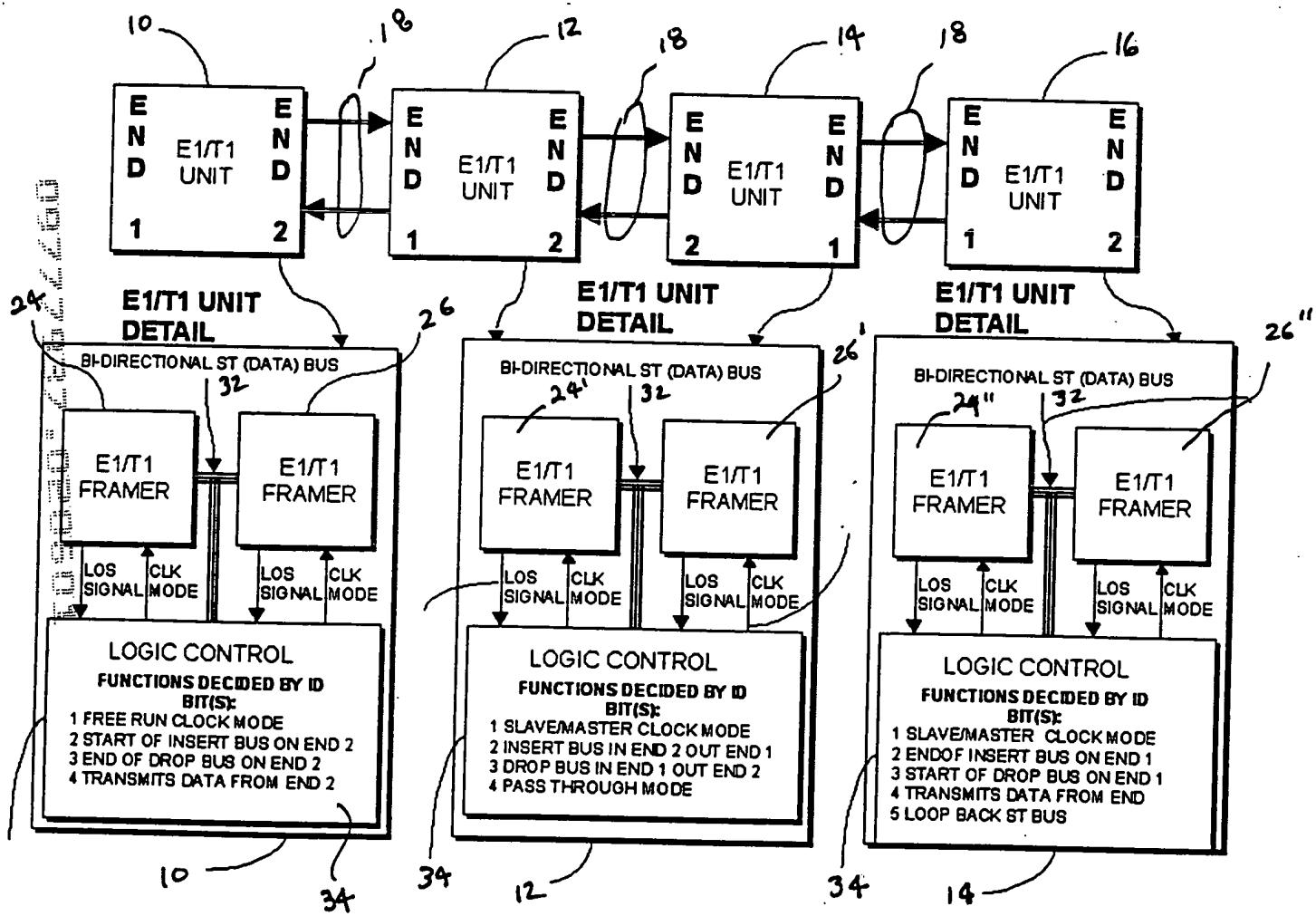
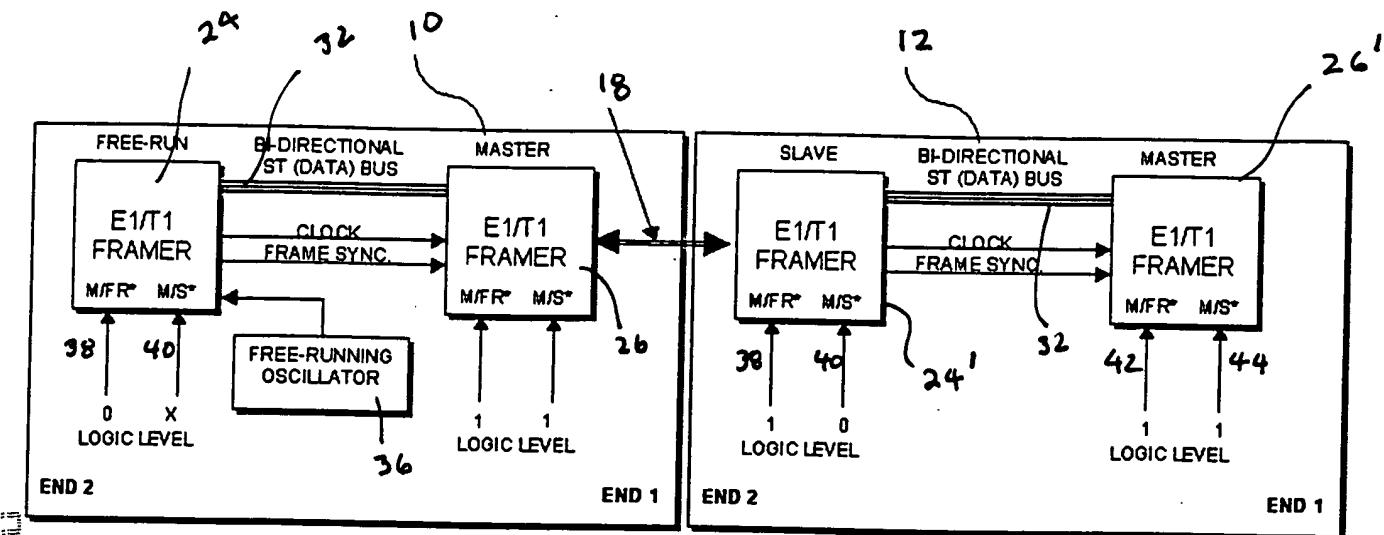


Fig. 2

FIG 3



## FRAMER CHIP MODE CONTROL TABLE

MODE	MASTER	FREE RUN	SLAVE	FREE RUN
0	1	0	1	0

LOGIC LEVEL

Fig. 3A

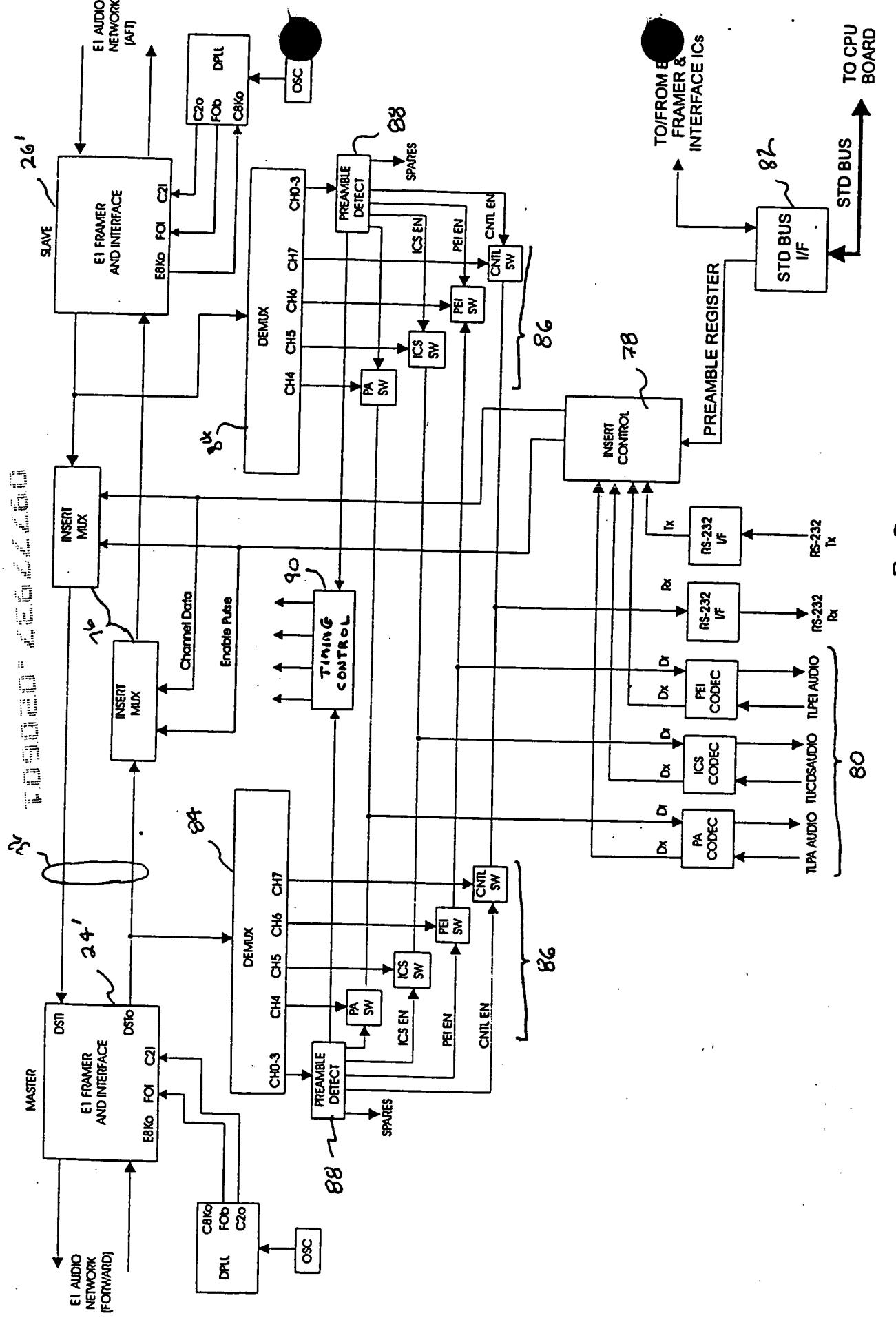


FIG. 4

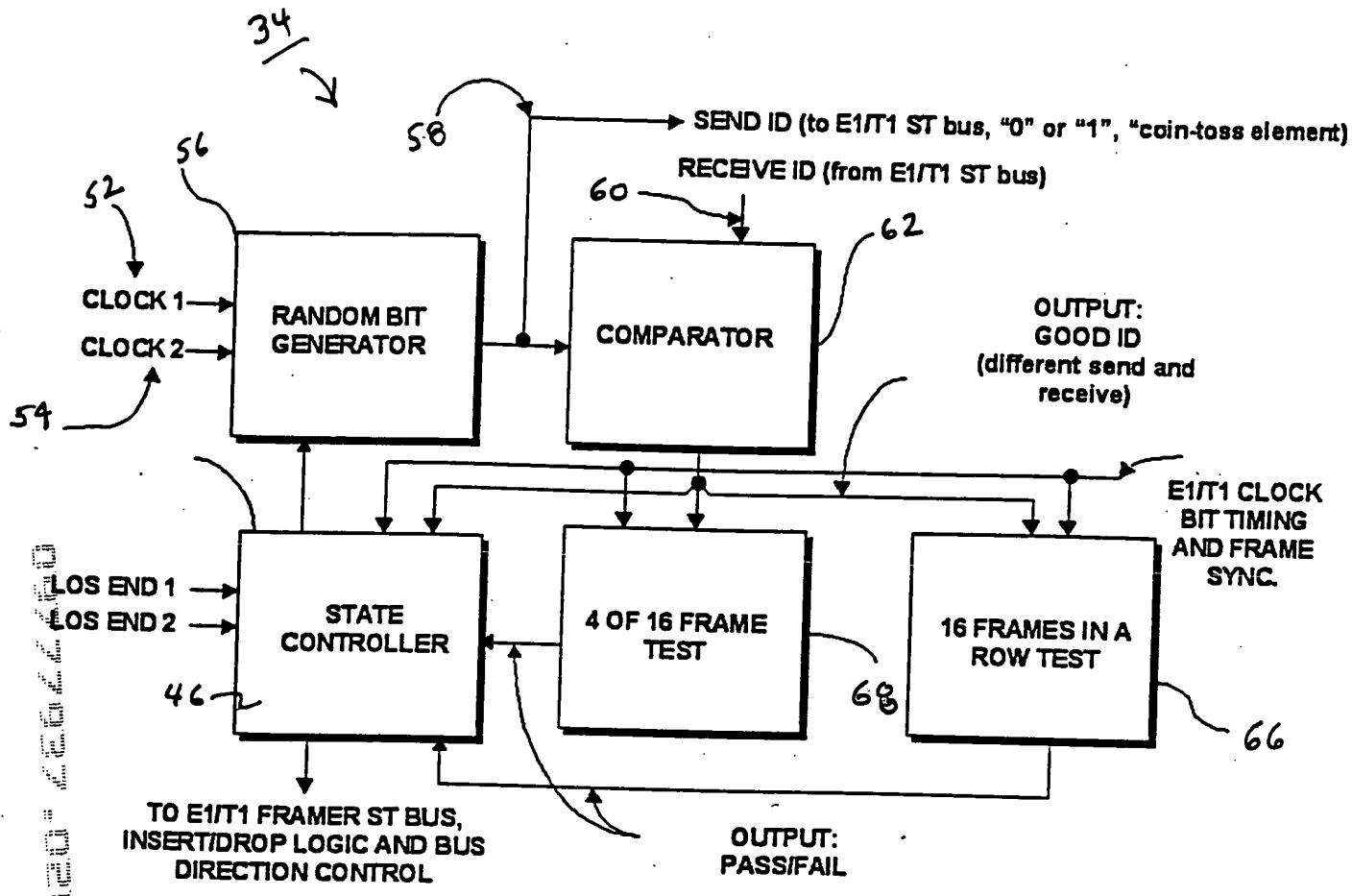


Fig. 5

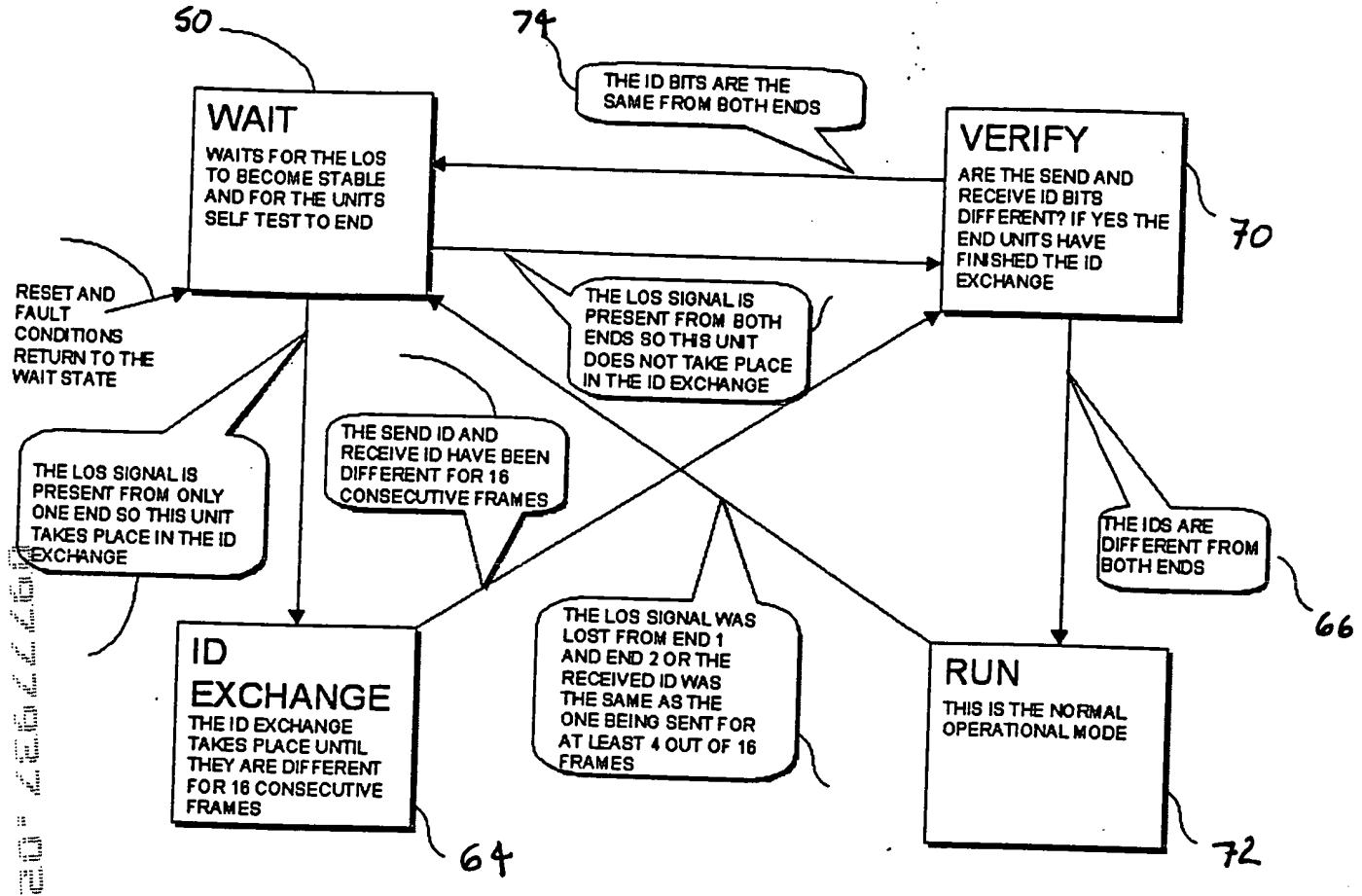


Fig. 6

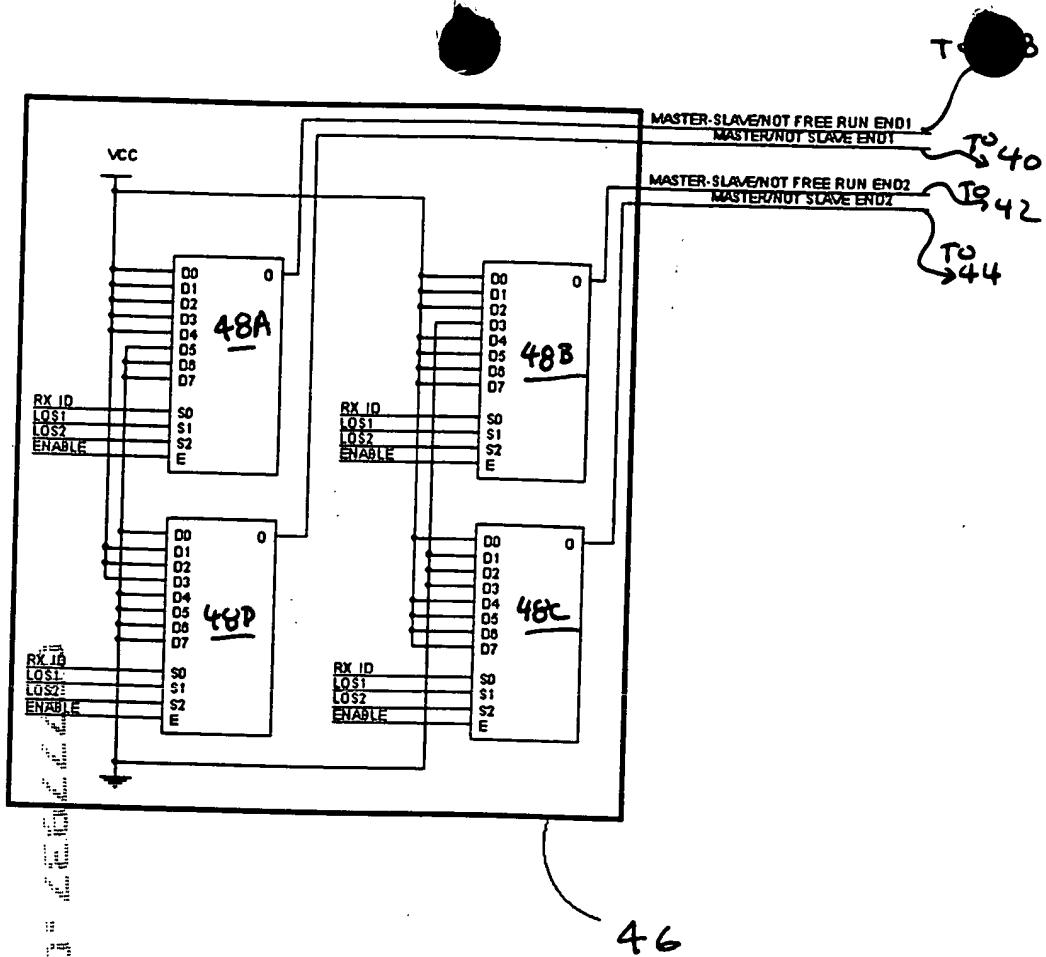


Fig. 7

Fig 7A

Mode Table

<u>LOS1</u>	<u>LOS2</u>	<u>Rx</u>	<u>Address</u>	<u>Master</u>	<u>Slave</u>	<u>Free-run</u>
0	0	0	0		end 2	end 1
0	0	1	1		end 1	end 2
0	1	0	2		end 1	end 2
0	1	1	3		end 1	end 2
1	0	0	4		end 2	end 1
1	0	1	5		end 2	end 1
1	1	0	6			
1	1	1	7			